TED (15) -3131

(REVISION — 2015)

Reg. No.....

Signature .....

DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/ MANAGEMENT/COMMERCIAL PRACTICE — OCTOBER, 2017

COMPUTER ARCHITECTURE

[*Time* : 3 hours

(Maximum marks : 100)

PART — A

(Maximum marks : 10)

Marks

I Answer all questions in one or two sentences. Each question carries 2 marks.

1. List the main structural components of a computer.
2. Define seek time.
3. Write the name of the registers that are essential for instruction execution.
4. List Flynn's classification of computer systems.
5. Define pipelining. (5×2 = 10)

PART — B

(Maximum marks : 30)

II Answer any *five* of the following questions. Each question carries 6 marks.

1. Explain the operations of a semi conductor memory cell with the help of neat sketches.
2. Write short note on High-Definition optical disk.
3. List and explain the operations that must be performed by the processor.
4. Explain functional requirements for the control unit.
5. Write short note on SDRAM.
6. List the major functions of I/O module.
7. Describe advantages and disadvantages of microprogramming. (5×6 = 30)

Marks

PART — C

(Maximum marks : 60)

(Answer *one* full question from each unit. Each full question carries 15 marks.)

UNIT — I

III (a) Explain Von Neuman machine with the help of a neat sketch. 8

(b) Compare static and dynamic RAM. 7

OR

IV (a) Explain associative mapping with the help of an example. 8

(b) Explain the elements of bus design. 7

UNIT — II

V (a) List and explain RAID levels. 8

(b) Explain interrupt driven I/O. 7

OR

VI (a) Explain the block diagram of an external device. 8

(b) Explain DVD. 7

UNIT — III

VII (a) Explain user-visible registers. 8

(b) Explain indirect cycle. 7

OR

VIII (a) Explain advantages and disadvantages of condition codes. 7

(b) Explain two-stage instruction pipelining with the help of a neat sketch. 8

UNIT — IV

IX (a) Explain hardwired implementation. 7

(b) Explain types of parallel processing systems. 8

OR

X (a) Explain fetch cycle. 7

(b) Draw and explain parallel processor organization. 8